ANALOG DEVICES

Low Distortion, Wide Bandwidth Voltage Feedback Clamp Amps

AD8036/AD8037

FEATURES

Superb Clamping Characteristics
- 3 mV Clamp Error
- 1.5 ns Overdrive Recovery
- Minimized Nonlinear Clamping Region
- 240 MHz Clamp Input Bandwidth
- ±3.9 V Clamp Input Range

Wide Bandwidth	AD8036	AD8037
Small Signal	240 MHz	270 MHz
Large Signal (4 V p-p)	195 MHz	190 MHz

Good DC Characteristics
- 2 mV Offset
- 10 μV/°C Drift

Ultralow Distortion, Low Noise
- –72 dBc typ @ 20 MHz
- 4.5 nV/√Hz Input Voltage Noise

High Speed
- Slew Rate 1500 V/μs
- Settling 10 ns to 0.1%, 16 ns to 0.01%

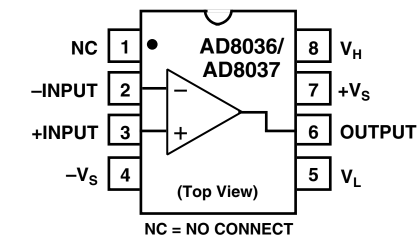
±3 V to ±5 V Supply Operation

APPLICATIONS

- ADC Buffer
- IF/RF Signal Processing
- High Quality Imaging
- Broadcast Video Systems
- Video Amplifier
- Full Wave Rectifier

FUNCTIONAL BLOCK DIAGRAM

8-Lead Plastic DIP (N), Cerdip (Q), and SO Packages



PRODUCT DESCRIPTION

The AD8036 and AD8037 are wide bandwidth, low distortion clamping amplifiers. The AD8036 is unity gain stable. The AD8037 is stable at a gain of two or greater. These devices allow the designer to specify a high (V_{CH}) and low (V_{CL}) output clamp voltage. The output signal will clamp at these specified levels. Utilizing a unique patent pending CLAMPIN™ input clamp architecture, the AD8036 and AD8037 offer a 10× improvement in clamp performance compared to traditional output clamping devices. In particular, clamp error is typically 3 mV or less and distortion in the clamp region is minimized. This product can be used as a classical op amp or a clamp amplifier where a high and low output voltage are specified.

The AD8036 and AD8037, which utilize a voltage feedback architecture, meet the requirements of many applications which previously depended on current feedback amplifiers. The AD8036 and AD8037 exhibit an exceptionally fast and accurate pulse response (16 ns to 0.01%), extremely wide small-signal and large-signal bandwidths and ultralow distortion. The AD8036 achieves –66 dBc at 20 MHz, and 240 MHz small-signal and 195 MHz large-signal bandwidths. The AD8036 and AD8037's recover from 2× clamp overdrive within 1.5 ns. These characteristics position the AD8036/AD8037 ideally for driving as well as buffering flash and high resolution ADCs.

In addition to traditional output clamp amplifier applications, the input clamp architecture supports the clamp levels as additional inputs to the amplifier. As such, in addition to static dc clamp levels, signals with speeds up to 240 MHz can be applied to the clamp pins. The clamp values can also be set to any value within the output voltage range provided that V_H is greater that V_L. Due to these clamp characteristics, the AD8036 and AD8037 can be used in nontraditional applications such as a full-wave rectifier, a pulse generator, or an amplitude modulator. These novel applications are only examples of some of the diverse applications which can be designed with input clamps.

The AD8036 is offered in chips, industrial (–40°C to +85°C) and military (–55°C to +125°C) package temperature ranges and the AD8037 in industrial. Industrial versions are available in plastic DIP and SOIC; MIL versions are packaged in cerdip.

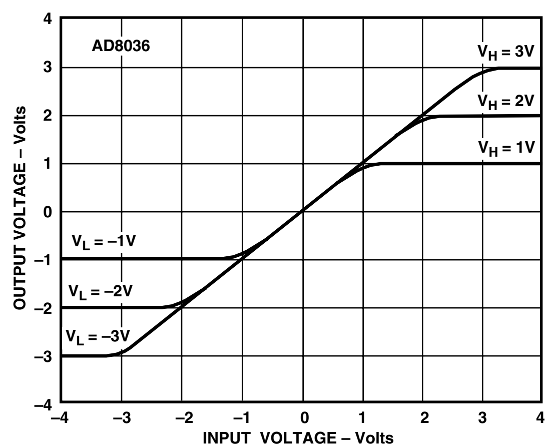


Figure 1. Clamp DC Accuracy vs. Input Voltage

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AD8036/AD8037–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = +1$ (AD8036); $A_V = +2$ (AD8037), V_H, V_L open, unless otherwise noted)

Parameter	Conditions	AD8036A Min	AD8036A Typ	AD8036A Max	AD8037A Min	AD8037A Typ	AD8037A Max	Unit
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	150	240		200	270		MHz
Large Signal[1]	8036, $V_{OUT} = 2.5$ V p-p; 8037, $V_{OUT} = 3.5$ V p-p	160	195		160	190		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} \le 0.4$ V p-p							
	8036, $R_F = 140\ \Omega$; 8037, $R_F = 274\ \Omega$		130			130		MHz
Slew Rate, Average +/–	$V_{OUT} = 4$ V Step, 10–90%	900	1200		1100	1500		V/µs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step, 10–90%		1.4			1.2		ns
	$V_{OUT} = 4$ V Step, 10–90%		2.6			2.2		ns
Settling Time								
To 0.1%	$V_{OUT} = 2$ V Step		10			10		ns
To 0.01%	$V_{OUT} = 2$ V Step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
2nd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–59	–52		–52	–45	dBc
	$R_L = 500\ \Omega$		–66	–59		–72	–65	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–68	–61		–70	–63	dBc
	$R_L = 500\ \Omega$		–72	–65		–80	–73	dBc
3rd Order Intercept	25 MHz		46			41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		6.7			4.5		$nV\sqrt{Hz}$
Input Current Noise	1 MHz to 200 MHz		2.2			2.1		$pA\sqrt{Hz}$
Average Equivalent Integrated								
Input Noise Voltage	0.1 MHz to 200 MHz		95			60		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.05	0.09		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	DC to 100 MHz		1.1			1.1		Degree
CLAMP PERFORMANCE								
Clamp Voltage Range[2]	V_{CH} or V_{CL}	±3.3	±3.9		±3.3	±3.9		V
Clamp Accuracy	2× Overdrive, $V_{CH} = +2$ V, $V_{CL} = -2$ V		±3	±10		±3	±10	mV
	$T_{MIN}–T_{MAX}$			±20			±20	mV
Clamp Nonlinearity Range[3]			100			100		mV
Clamp Input Bias Current (V_H or V_L)	8036, $V_{H,L} = \pm 1$ V; 8037, $V_{H,L} = \pm 0.5$ V		±40	±60		±50	±70	µA
	$T_{MIN}–T_{MAX}$			±80			±90	µA
Clamp Input Bandwidth (–3 dB)	V_{CH} or $V_{CL} = 2$ V p-p	150	240		180	270		MHz
Clamp Overshoot	2× Overdrive, V_{CH} or $V_{CL} = 2$ V p-p		1	5		1	5	%
Overdrive Recovery	2× Overdrive		1.5			1.3		ns
DC PERFORMANCE[4], $R_L = 150\ \Omega$								
Input Offset Voltage[5]			2	7		2	7	mV
	$T_{MIN}–T_{MAX}$			11			10	mV
Offset Voltage Drift			±10			±10		µV/°C
Input Bias Current			4	10		3	9	µA
	$T_{MIN}–T_{MAX}$			15			15	µA
Input Offset Current			0.3	3		0.1	3	µA
	$T_{MIN}–T_{MAX}$			5			5	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2$ V	66	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	48	55		54	60		dB
	$T_{MIN}–T_{MAX}$	40			46			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±2.5			±2.5		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			20.5	21.5		18.5	19.5	mA
	$T_{MIN}–T_{MAX}$			25			24	mA
Power Supply Rejection Ratio	$T_{MIN}–T_{MAX}$	50	60		56	66		dB

NOTES

[1]See Max Ratings and Theory of Operation sections of data sheet.

[2]See Max Ratings.

[3]Nonlinearity is defined as the voltage delta between the set input clamp voltage (V_H or V_L) and the voltage at which V_{OUT} starts deviating from V_{IN} (see Figure 73).

[4]Measured at $A_V = 50$.

[5]Measured with respect to the inverting input.

Specifications subject to change without notice.

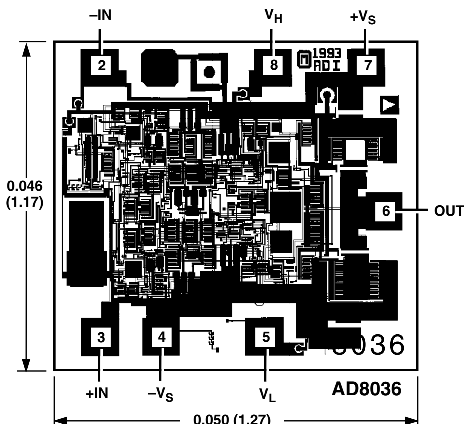
ABSOLUTE MAXIMUM RATINGS[1]

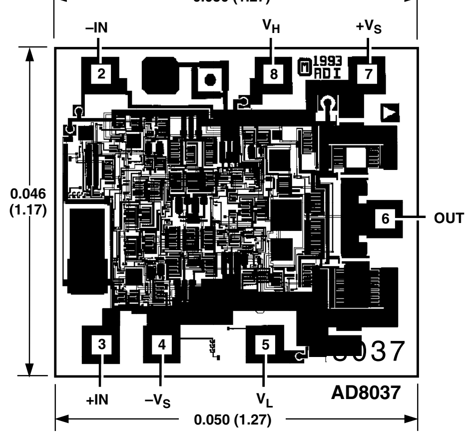
Supply Voltage . . . . 12.6 V
Voltage Swing × Bandwidth Product . . . . 350 V-MHz
$|V_H–V_{IN}|$ . . . . ≤ 6.3 V
$|V_L–V_{IN}|$ . . . . ≤ 6.3 V
Internal Power Dissipation[2]
  Plastic DIP Package (N) . . . . 1.3 Watts
  Small Outline Package (SO) . . . . 0.9 Watts
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±1.2 V
Output Short Circuit Duration
  . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic DIP: θ_{JA} = 90°C/W
8-Lead SOIC: θ_{JA} = 155°C/W
8-Lead Cerdip: θ_{JA} = 110°C/W.

METALIZATION PHOTO

Dimensions shown in inches and (mm).
Connect Substrate to $-V_S$.





MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8036 and AD8037 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

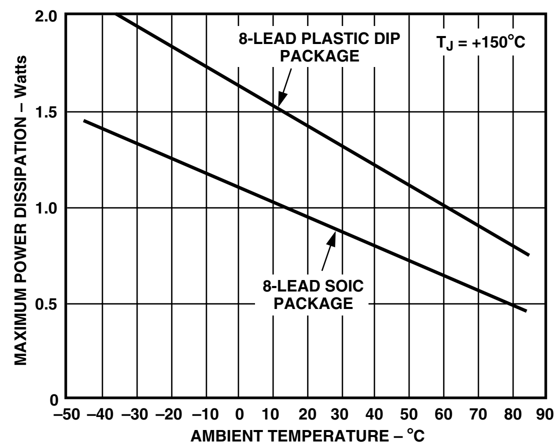


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8036AN	–40°C to +85°C	Plastic DIP	N-8
AD8036AR	–40°C to +85°C	SOIC	SO-8
AD8036AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8
AD8036AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8
AD8036ACHIPS	–40°C to +85°C	Die	
AD8036-EB		Evaluation Board	
5962-9559701MPA	–55°C to +125°C	Cerdip	Q-8
AD8037AN	–40°C to +85°C	Plastic DIP	N-8
AD8037AR	–40°C to +85°C	SOIC	SO-8
AD8037AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8
AD8037AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8
AD8037ACHIPS	–40°C to +85°C	Die	
AD8037-EB		Evaluation Board	

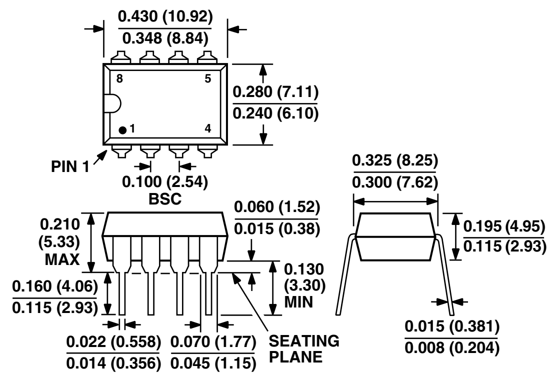
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8036/AD8037 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

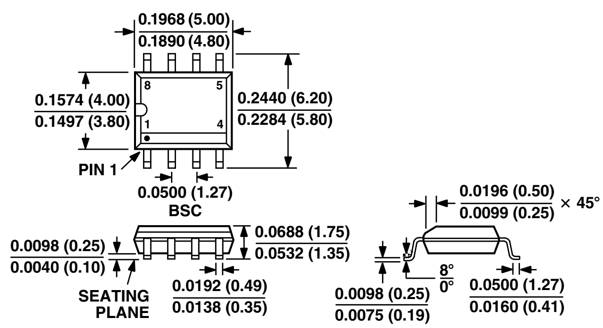
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

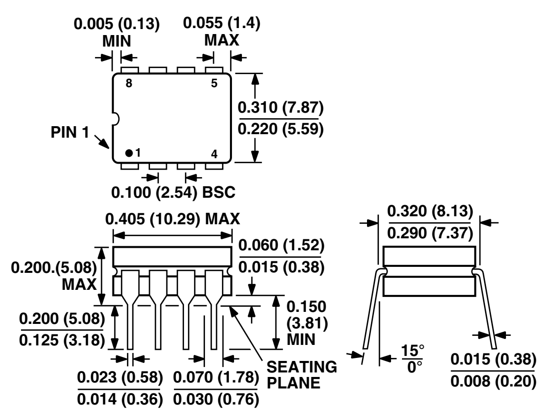
8-Lead Plastic DIP (N Package)



8-Lead Plastic SOIC (SO Package)



8-Lead Cerdip (Q Package)



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